DLD

EXPERIMENT – 8

Aim: To simulate the logic gates of 8bit shift registers

Tools used: vivado software

Truth table:

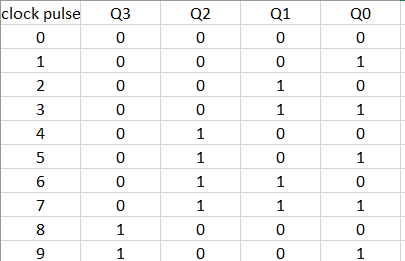
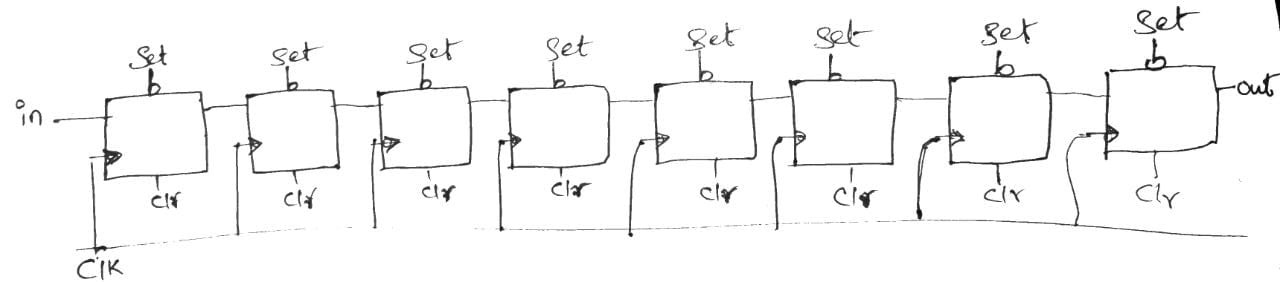
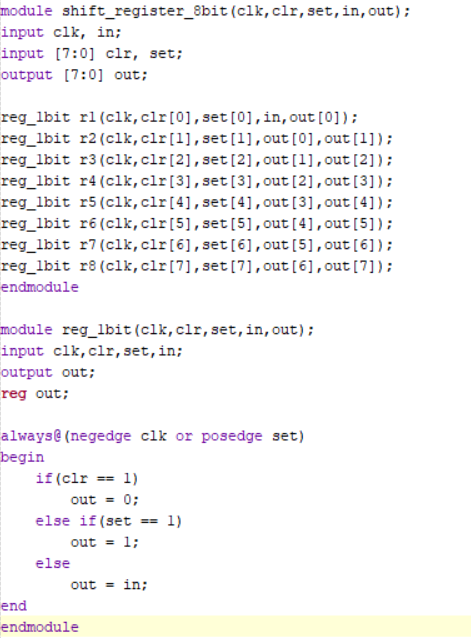


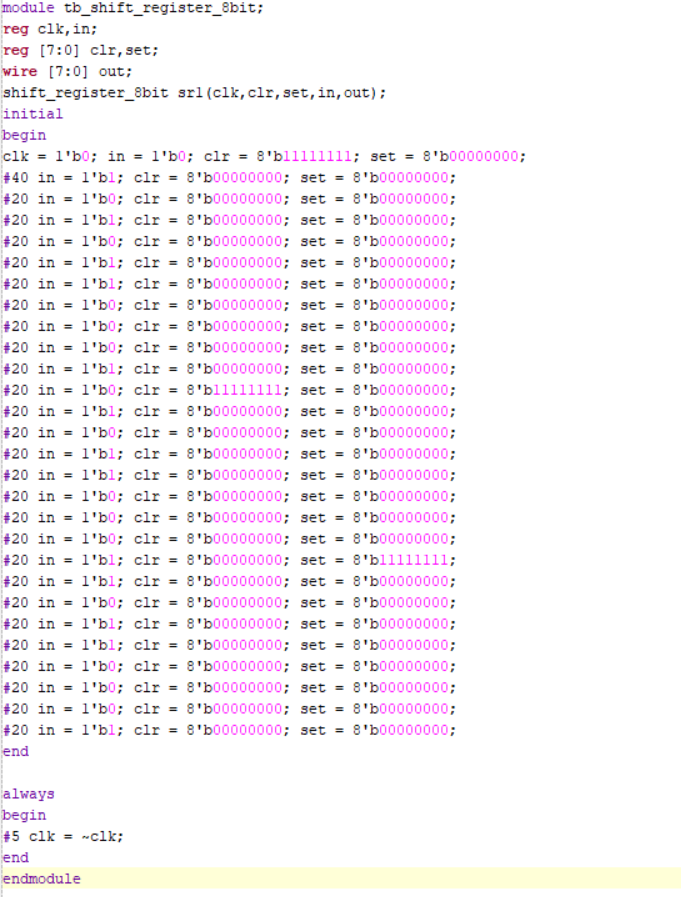
Diagram:



Verilog codes:

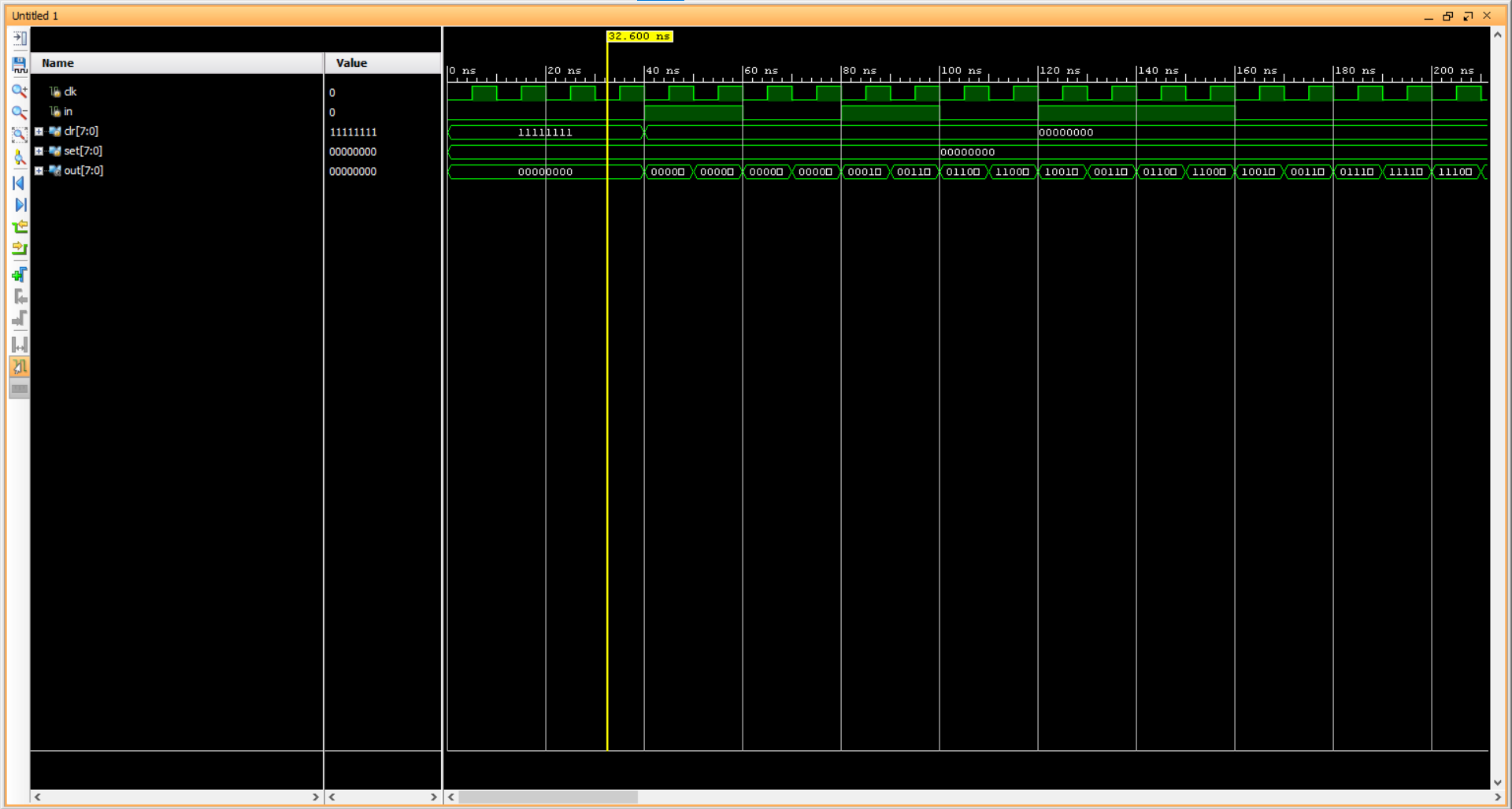


Test bench code:



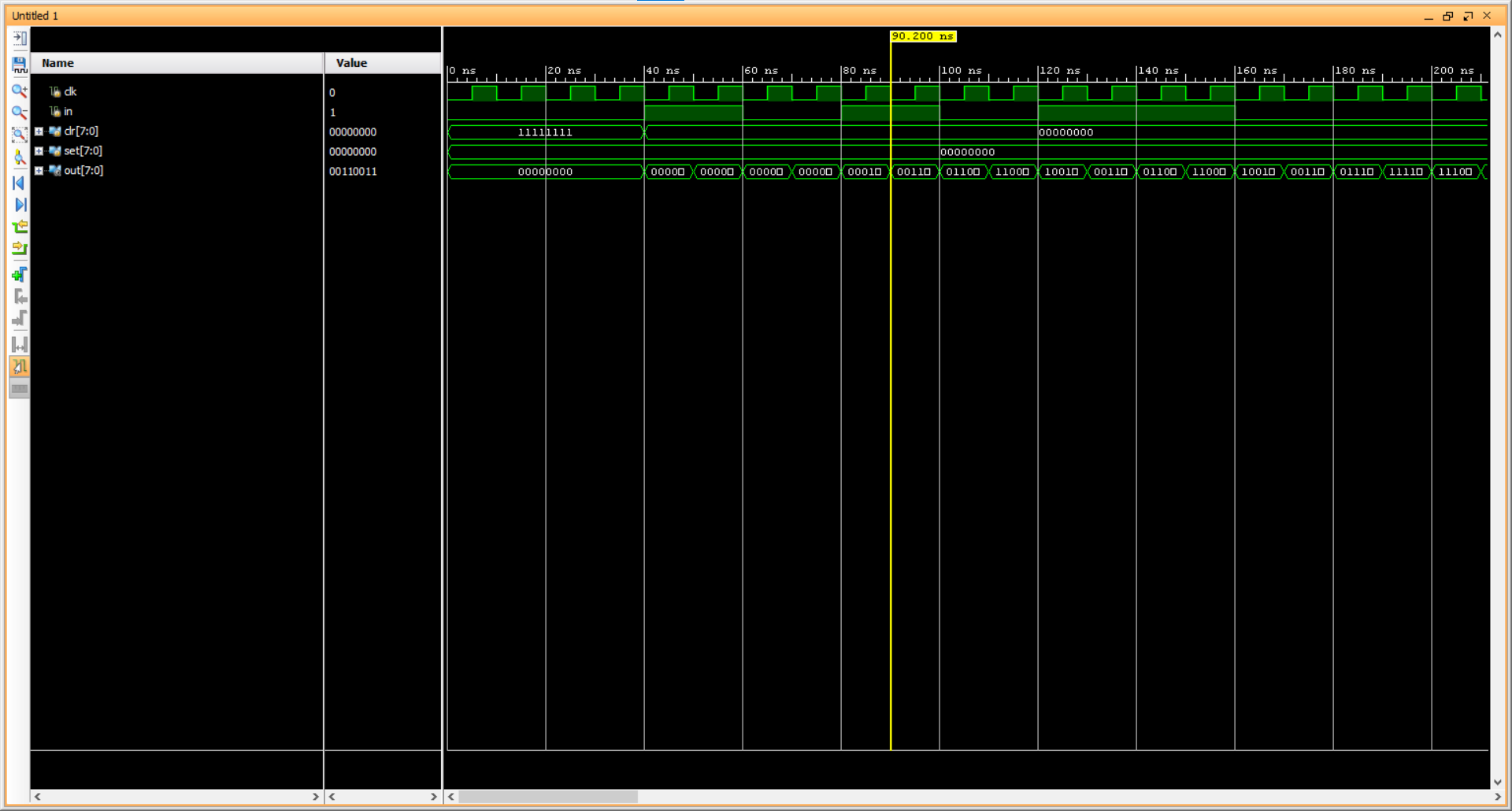
Outputs:

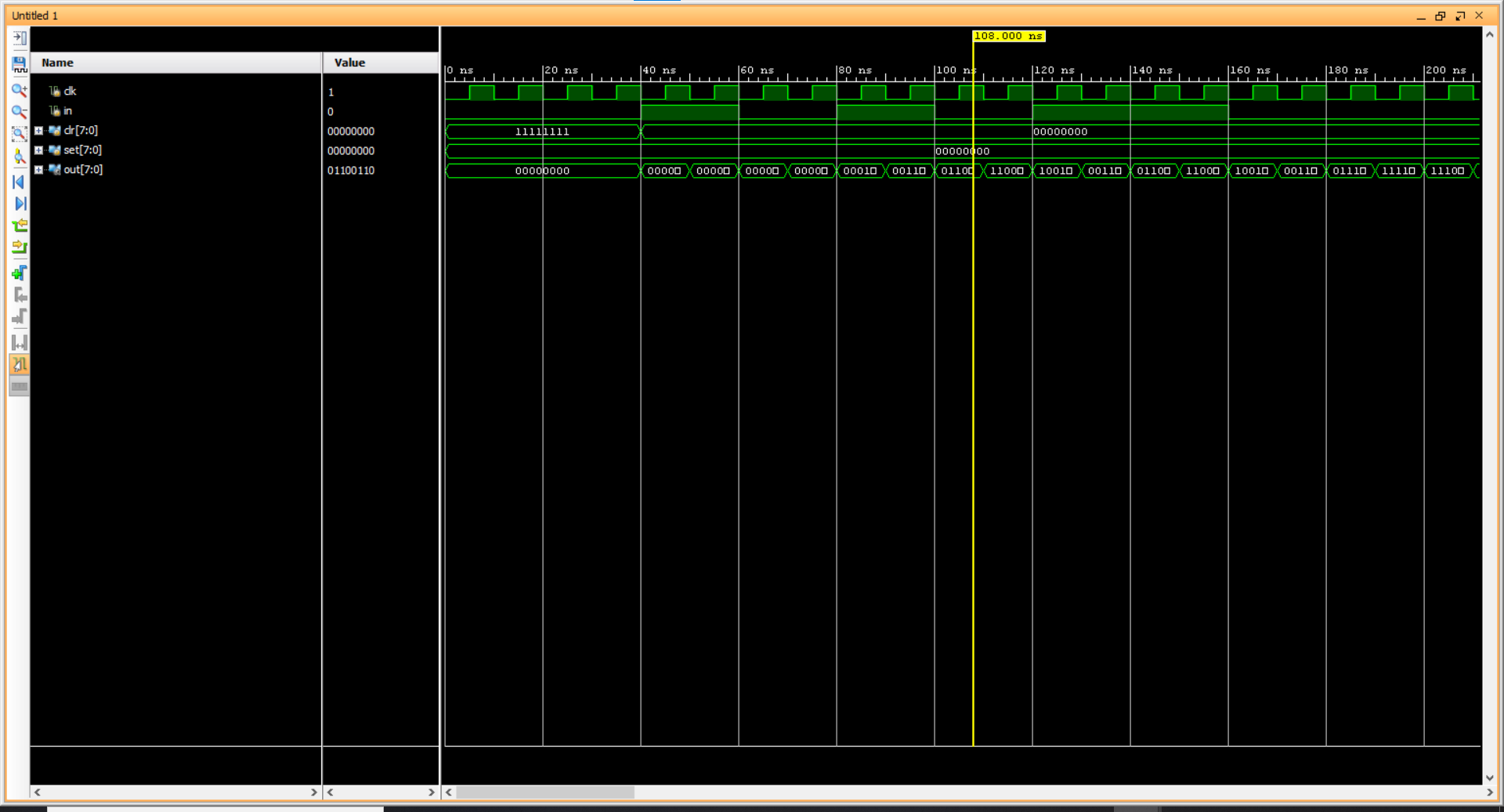


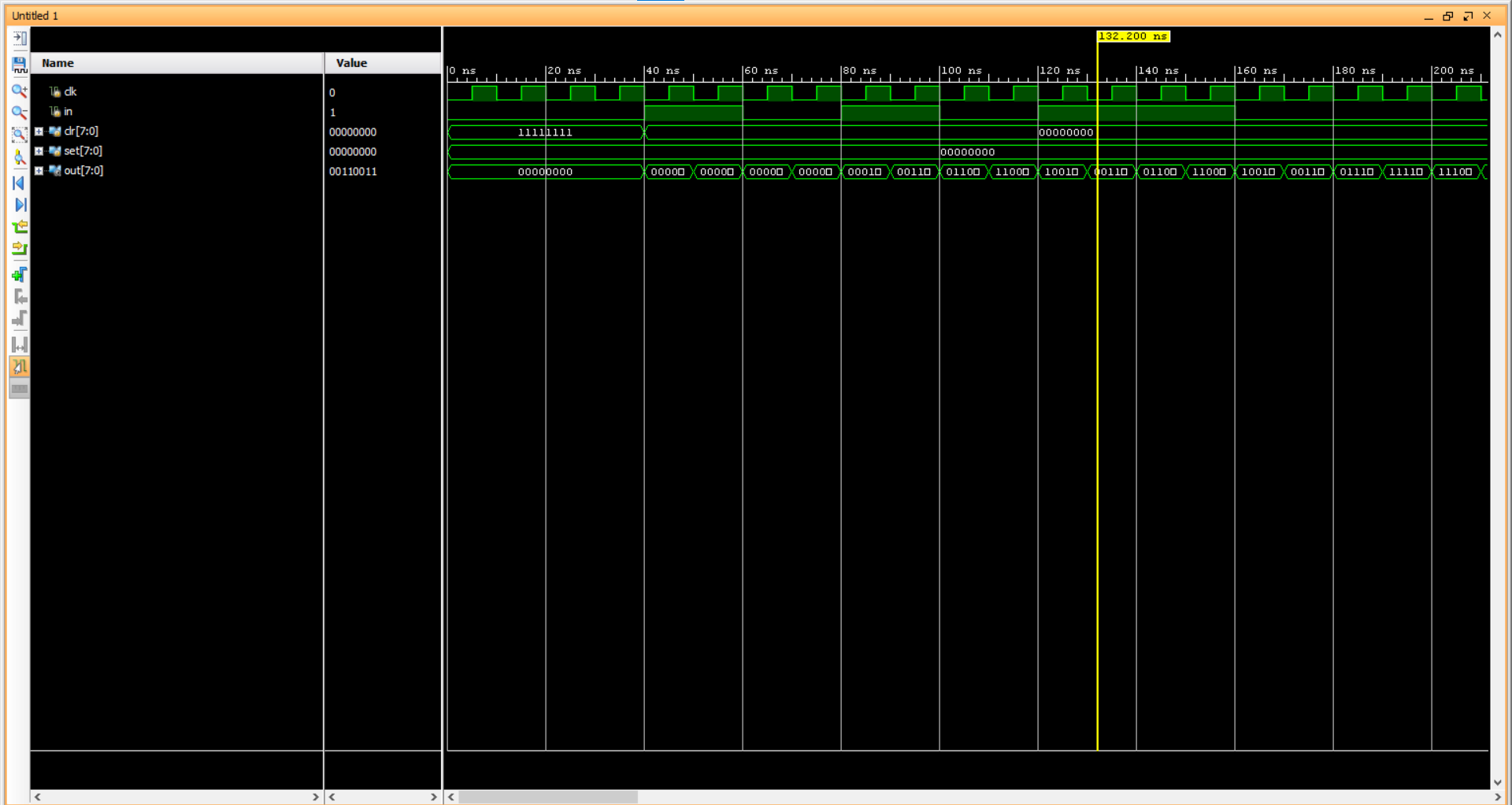


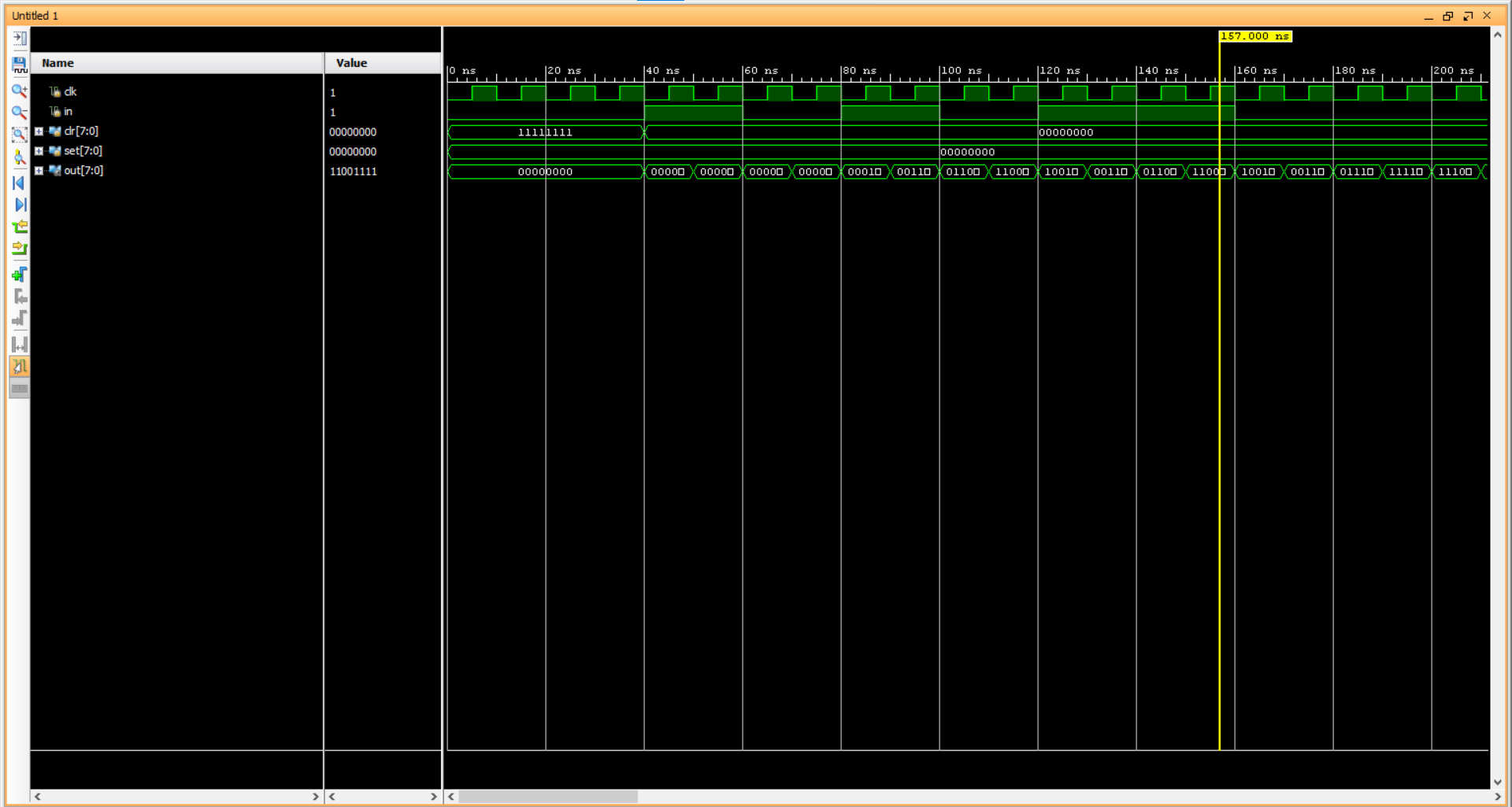


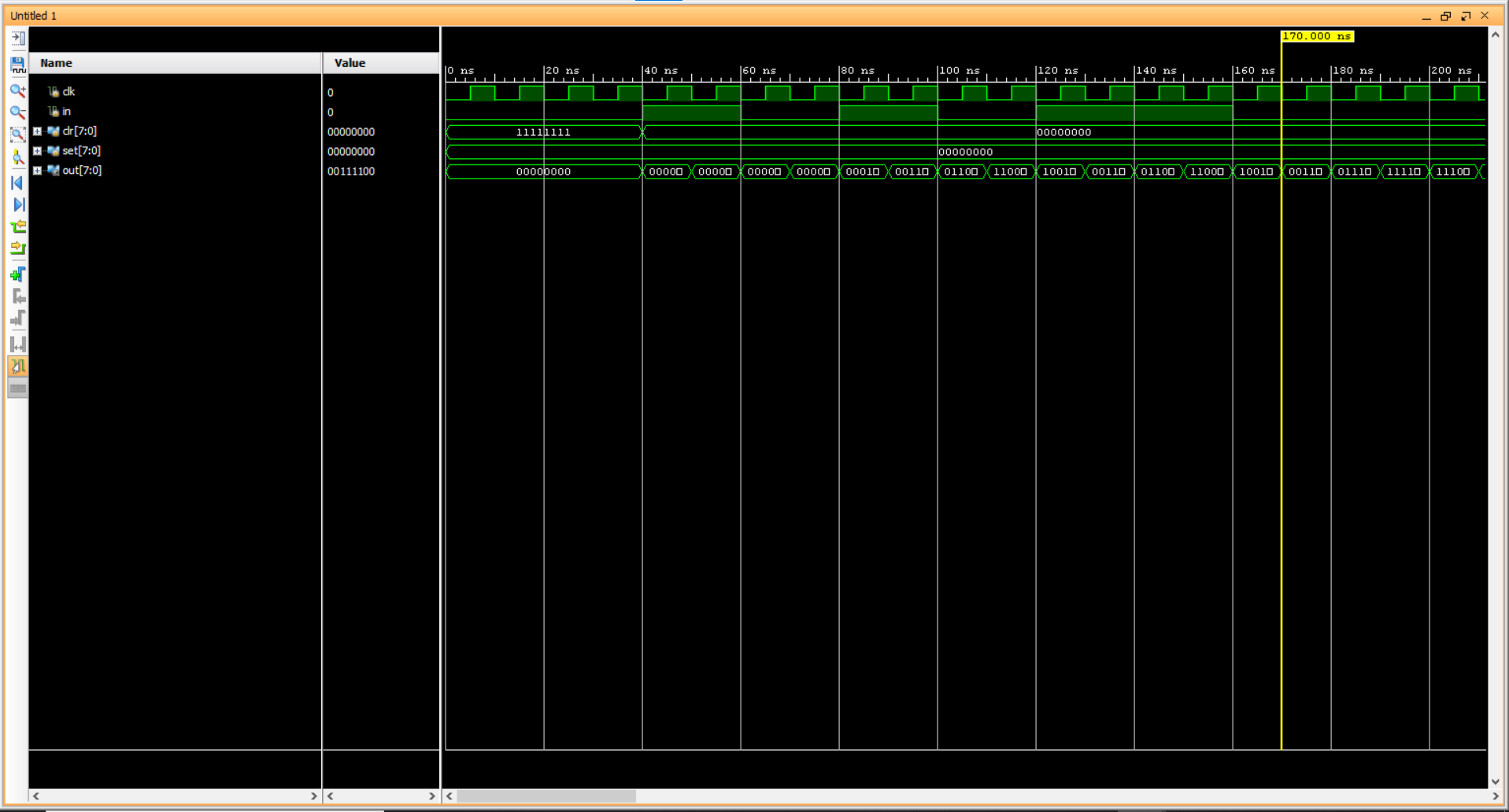


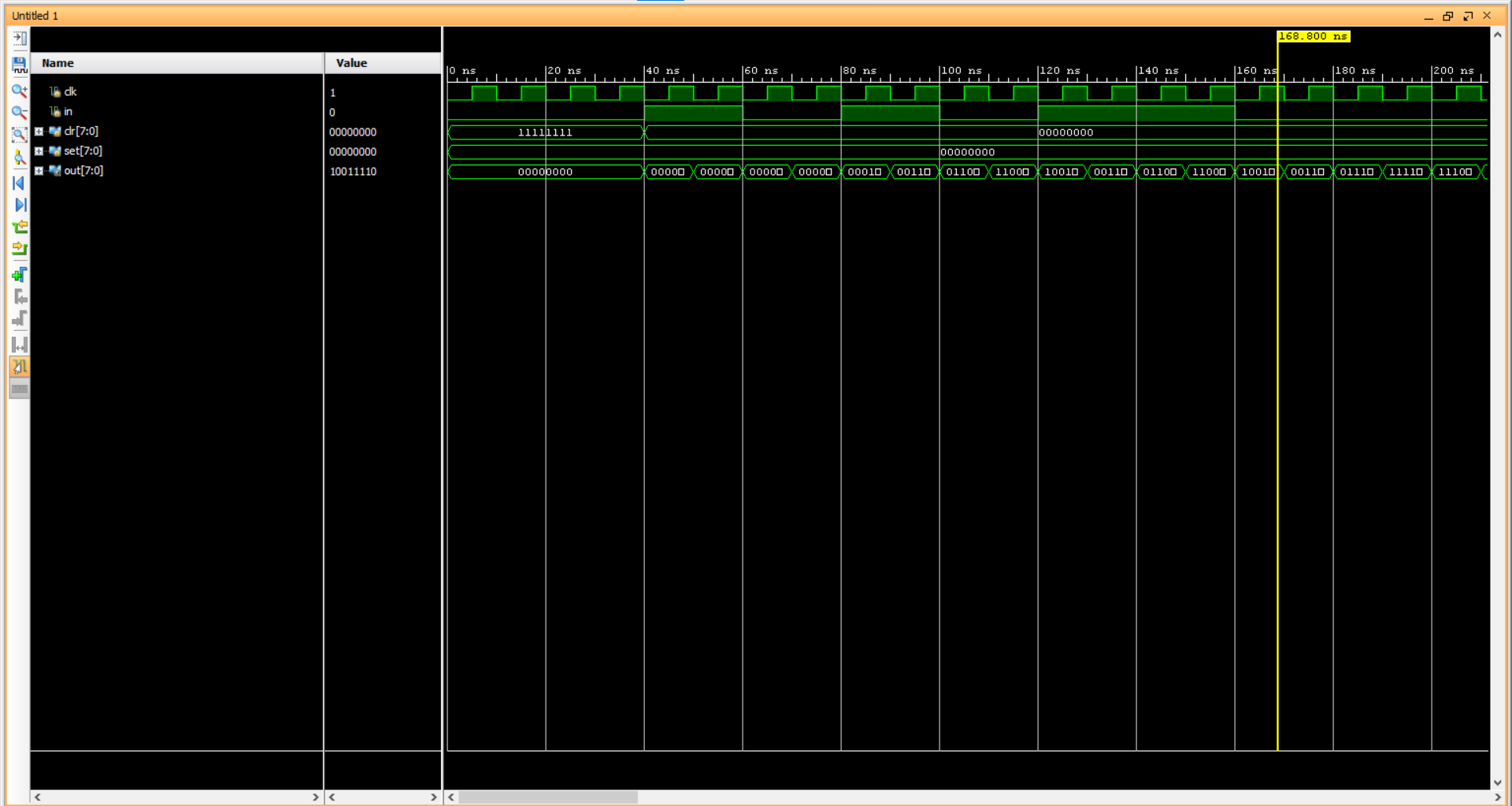


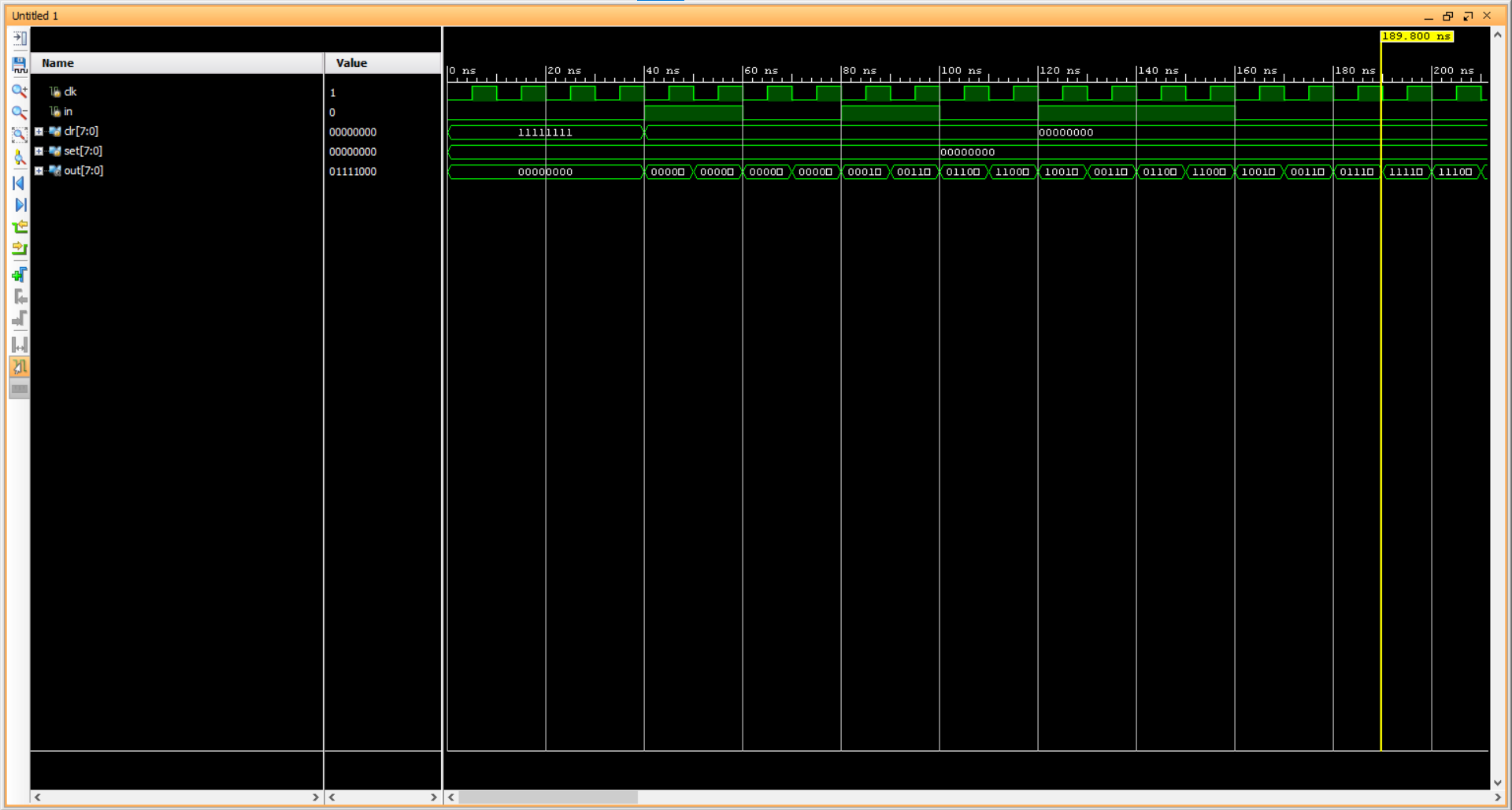


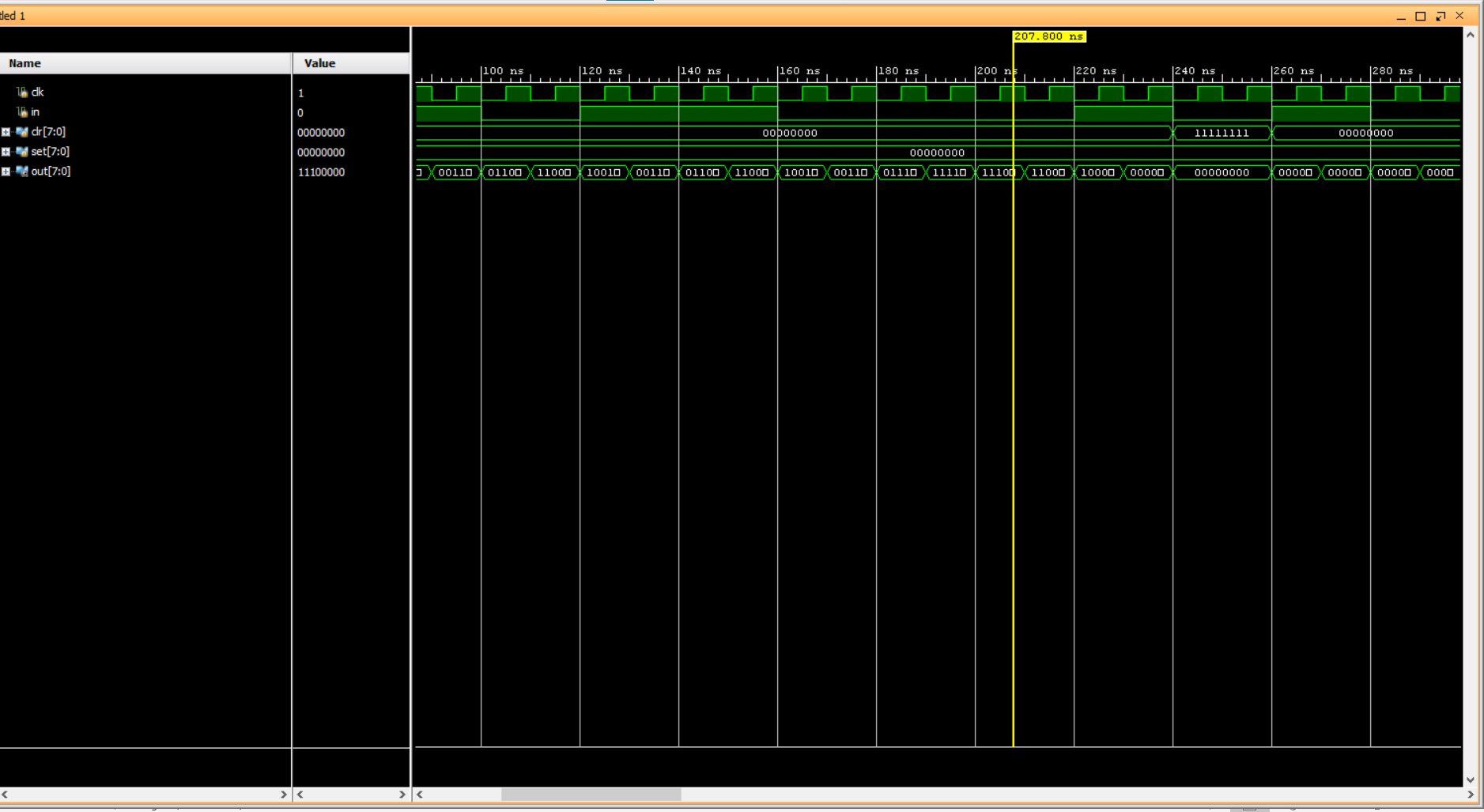












Conclusion: In this lab I’m now able write shift register